Attorney Docket No. 73510 (7114)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appln No.:	09/862,391
Applicants:	Milne, James R. et. al
Filed:	May 21, 2001
For:	MODULAR DIGITAL TELEVISION ARCHITECTURE
TC/A.U.:	2622
Examiner:	Yenke, Brian P.

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AMENDED APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Pursuant to 37 C.F.R. §1.192, and in response to the "Notification of Non-Compliant Appeal Brief" mailed on April 13, 2007, the Applicants hereby respectfully submit the following Amended Appeal Brief in support of their appeal. This Amended Appeal Brief replaces the original brief filed on February 20, 2007.

(1) Real Party in Interest

The real parties in interest are (a) Sony Corporation, a Japanese corporation having a primary place of business in Tokyo, Japan; and (b) Sony Electronics Inc., a U.S. corporation having a primary place of business in Park Ridge, New Jersey.

(2) Related Appeals and Interferences

The present application is a parent application of application Serial No. 10/112,228, which was filed on March 28, 2002. An appeal of application Serial No. 10/112,228 is also presently pending before this Board.

(3) Status of Claims

Claims 1-13, which constitute the subject matter of this appeal, are pending. All of the claims are under final rejection.

(4) Status of Amendments

No amendments have been submitted subsequent to the Final Rejection in this application.

(5) Summary of Claimed Subject Matter

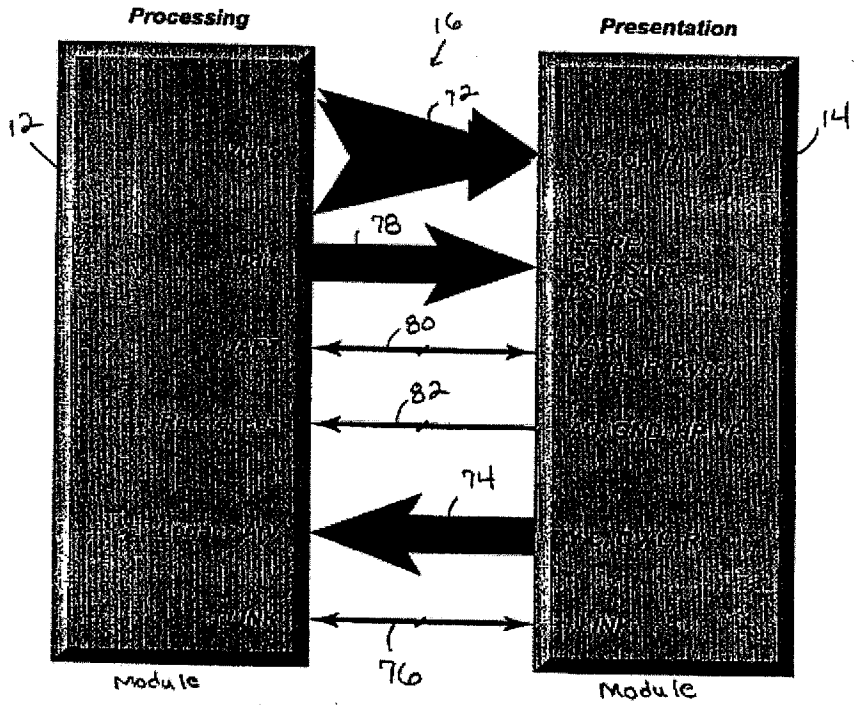
In the pending application, claims 1-13 are pending. Claims 1, 9, and 11 are independent apparatus claims. The remaining claims depend directly or indirectly upon these independent claims.

In previous television systems, the hardware components of the system were designed first. After the design of the hardware components was completed and certified, the software protocols used to implement the functionalities of the system were then developed. Thus, because of the order of the design process, previous systems required the grouping of software protocols to a specific hardware configuration.

These previous approaches had several disadvantages. For example, due to the one-to-one correspondence between the hardware and software components, any change in the design of the hardware required that completely new software be developed. Interchanging components between different systems was also generally not possible. Additionally, the ability to upgrade or enhance the operational capabilities of the hardware design with new software was not possible.

The Applicants' invention addresses the shortcomings and limitations of previous systems. More specifically, claim 1 recites a digital television architecture that includes a

processing chassis (e.g., processing chassis 12 as shown in FIG. 4 of the application and which is reproduced below for the convenience of the reader). The processing chassis (e.g., processing chassis 12) is operative to convert an analog input signal into at least a first digital signal for use in providing information to a user. Specification, page 4, lines 9-17. The processing chassis (e.g., processing chassis 12) includes a dedicated power source and processing element. Specification, page 5, lines 11-13. The architecture also includes a presentation chassis (e.g., presentation chassis 14 as shown in FIG. 4) that is operative to convert audio and visual components of the at least first digital signal into a final signal for presentation on a display.



The audio and visual conversion are performed in a first domain and the presentation device chassis (e.g., presentation chassis 14) is separate from the processing chassis (e.g., processing chassis 12) and includes a dedicated power source of the presentation chassis (e.g., presentation chassis 14) that is different from the power source of the processing chassis (e.g., processing chassis 12). Specification, page 14, lines 20-31. The architecture also includes a global interface (e.g., global interface 16) that is operative to provide a technology-independent communication path between the processing chassis (e.g., processing chassis 12) and the presentation chassis (e.g., presentation chassis 14). Specification, page 12, lines 9-26.

Independent claim 9 recites a modular television architecture that includes a processing module (e.g., processing chassis 12). The processing module (e.g., processing chassis 12) includes circuitry operative to convert an input signal from a first type into at least a second type. Specification, page 4, lines 9-17. The conversion is performed in the digital domain. The architecture includes a presentation module (e.g., presentation chassis 14) that is operative to convert audio and visual information contained within the at least second signal into a final signal for presentation on a display device. The audio and visual conversion is performed in a first domain. The presentation module (e.g., presentation chassis 14) is separate from and operates independently of the processing module (e.g., processing chassis 12). See Specification, page 14, lines 20-31. The architecture also includes a global interface (e.g., global interface 16) that is operative to provide a technology-independent communication path between the processing module (e.g., processing chassis 12) and the presentation module (e.g., presentation chassis 14). See Specification, page 12, lines 9-26.

Independent claim 11 recites a television system that includes a processing module (e.g., processing chassis 12). The processing module (e.g., processing chassis 12) provides signals that represent information to be provided on a suitable display device. Specification, page 4, lines 9-17. The system also includes a presentation module (e.g., presentation chassis 14) that includes decoding and filtering elements that are operative to process the signals provided by the processing module and display the images represented on the display device. Specification, page 13, line 6- page 14, line 31. The presentation module (e.g., presentation chassis 14) is separate from and operates independently of the processing module (e.g.,

processing chassis 12). Specification, page 14, lines 20-31. The system also includes a global interface module (e.g., global interface 16) that couples the processing module and the presentation module (e.g., presentation chassis 14) together using a technology-independent path. Specification, page 12, lines 9-26. The processing module (e.g., processing chassis 12) and presentation module (e.g., presentation chassis 14) operate independently from one another and the processing performed by the processing module (e.g., processing chassis 12) is performed in the digital domain.

Consequently, because of the use of the global interface, the processing chassis and the presentation chassis can operate independently from each other. Families of digital televisions can be created by interchanging various combinations of processing and presentation modules with the global interface. See, Specification, page 15, lines 3-17.

(6) Grounds of Rejection to be Reviewed on Appeal

(A) Whether Claims 9 and 11-12 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent No. 6,340,994 to Margulis in view of U.S. Patent No. 6,469,742 to Trovato?

(B) Whether Claims 1-8, 10, and 13 are unpatentable under 35 U.S.C. §103(a) over Margulis in view of Trovato and U.S. Patent No. 6,469,742 to Phillips?

(7) Argument

(A) Claims 9 and 11-12 are Not Unpatentable under 35 U.S.C. §103(a) over Margulis in view of Trovato

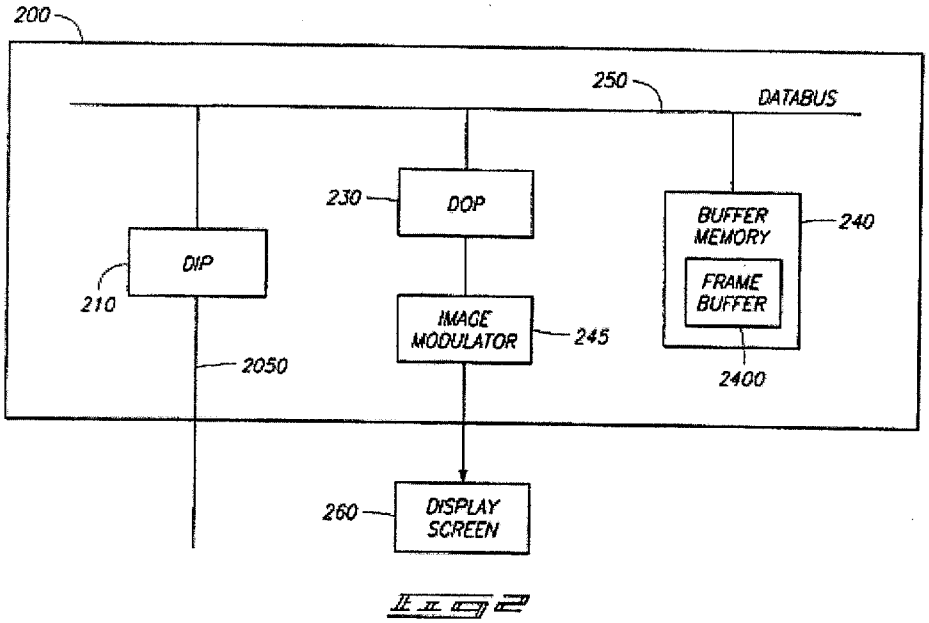
Claim 9 is Allowable because the Proposed Combination does not Teach or Suggest a Presentation Module that forms a Final Signal

As mentioned above, claim 9 recites a modular television architecture that includes a processing module. The processing module includes circuitry operative to convert an input signal from a first type into at least a second type. The conversion is performed in the digital domain. The architecture includes a presentation module that is operative to convert audio

and visual information contained within the at least second signal into a final signal for presentation on a display device. The audio and visual conversation is performed in a first domain. The presentation module is separate from and operates independently of the processing module. The architecture also includes a global interface that is operative to provide a technology-independent communication path between the processing module and the presentation module.

Margulis teaches approaches for enhancing the quality of digital images by geometrically transforming these images. As shown in FIG. 2 of Margulis (reproduced below for the convenience of the reader), a image processing system 200 includes a Display Input Processor (DIP) 210 that receives images on an input line 2050 and reconstructs the received images both spatially and temporally. Margulis, col. 6, lines 53- col. 7, line 18. The DIP 210 then transmits the images to a Digital Output Processor (DOP) 230 over a data bus 250. *Id.*

As seen in FIG. 2 of Margulis, the data bus 250 is an internal bus that is coupled to a memory 240. The DOP 230 enhances the visual quality of the images by geometrically transforming the images. *Id.* Next, the DOP sends the images to an image modulator 245, which modulates the geometrically transformed images and provides the modulated images to a display screen 260 to be presented to a user. *Id.*



The Examiner stated that the DOP 230 is a presentation module that forms a final signal for display as recited in claim 9. The Applicants respectfully disagree with this statement for the reasons stated below.

Specifically, the DOP 230 does not form a final signal for display. In fact, the image modulator 245 must perform additional processing (e.g., modulation functions) on the signal output by the DOP 230 to form a displayable signal. For this reason, the Applicants assert that the proposed combination does not include an element of claim 9 and that claim 9 is allowable for this reason.

Claim 9 is Allowable Because There is No Motivation to Modify Margulis as Suggested by the Examiner to Include a Global Interface

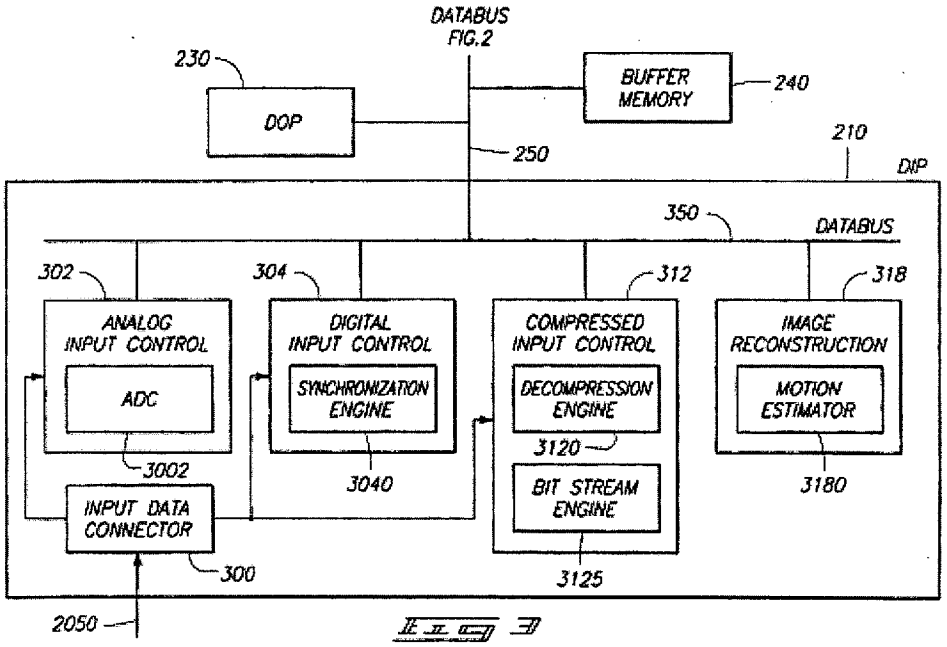
In rejecting the claim 9, the Examiner stated that:

> Regarding the [] limitation of global interface with technology-independent communication. Margulis discloses the interfaces/modules which use a high speed digital data transmission technique as that described in IEEE 1394 (i.e. plug an play, different modules/devices being able to

> communicate on the high speed data path). Also, as disclosed by applicant's own specification, this limitation is met by established standards such as DVI or EIA 861, thus since Margulis discloses the concept of interfacing using an established connection such as 1394, the use of DVI or EIA-861 are other standards available by the user/designer since each standard offers it's own advantages respectively, and the selection of such derives no unexpected results.

In other words, the Examiner apparently argues that because Margulis allegedly shows interfacing according to the IEEE 1394 standard, the proposed Margulis-Trovato combination can be modified to use a global interface (using any and all types of standards) at any location in the proposed system including at the DIP/DOP interface. The Applicants respectfully disagree with the Examiner's statements and assert that claim 9 is allowable over the proposed combination for the following reasons.

As shown in FIG. 3 of Margulis (reproduced below for the convenience of the reader), the DIP 210 includes a Digital Input Control 304 with a Synchronization Engine 3040. The Digital Input Control 304 uses a specific standard (e.g., the Institute of Electrical and Electronics Engineering (IEEE) standard 1394, Low Voltage Differential Signaling (LVDS) techniques, or Panel Link approaches) to ensure that it has properly ***received*** information over the input line 2050. *Id.* at col. 8, lines 9-20. The standards used by the Digital Input Control 304 relate to "line termination, voltage control, data formatting, phase lock loops (PLLs) and data recovery ***to assure that the Digital Input Control 304 properly receives the input data.***" *Id.* at col. 8, lines 18-20. Thus, a standardized interface is provided ***at the input*** of the DIP 210, ***not at the output*** of the DIP 210 (i.e., between the DIP 210 and the DOP 230).



It is not clear from the Examiner's remarks as to whether the Examiner is suggesting that while the DIP/DOP interface may not be standardized, it can be modified to include a global interface. Alternatively, it is not clear whether the Examiner is asserting that the DIP/DOP interface is standardized and for that reason can be modified to be a global interface to handle all types of communications.

If the Examiner is suggesting that the DIP/DOP interface is not standardized but can be modified to be a global interface, the Applicants respectfully disagree with this assertion. Specifically, the DIP/DOP interface handles internal communications of the system over the bus 250 (i.e., between components designed to communicate with each other). For this reason, there would be absolutely no benefit to converting the bus 250 to be a global interface. To the contrary, converting the bus 250 to be a global interface would require additional hardware and/or software support and significantly slow communication along the bus 250.

On the other hand, even if the DIP-DOP interface were somehow found to operate according to a particular standard, there is still no motivation to make the modification

suggested by the Examiner. Specifically, the DIP 210 ***already receives*** the input data in a fixed, first standard (e.g., IEEE 1394). The DOP 230 then processes the data to enhance the image quality. There would be no reason or benefit to using a DIP and a DOP that operate according to completely different standards (thereby requiring a global interface). Changing standards between the DIP 210 and DOP 230 would result in inevitable delays and potential processing errors. In fact, in order to avoid these problems, there would be every motivation to keep the same standards as between the DIP 210 and DOP 230.

There must be a suggestion in the reference or apparent to one skilled in the art to undertake the suggested modification. MPEP § 2143.01. In other words, it is improper for the Examiner to parse through the prior art to find the elements of the Applicants' claims and then use the Applicants' own teachings to combine the elements as claimed.

For these reasons, the Applicants assert that there is no motivation to make the Examiner's suggested modification to the Margulis reference and that claim 9 is allowable over the proposed Margulis-Trovato combination.

Claim 9 is Allowable Because the Proposed Modification Would Render Margulis Inoperative for Its Intended Purpose

Whether the connection between the DIP and the DOP is standardized or non-standardized, making the modification as suggested by the Examiner would render Margulis inoperative for its intended purpose. A proposed modification can not render the prior art unsatisfactory for its intended purpose. See MPEP § 2143.01.

In fact, modifying the interface between the DIP 210 and DOP 230 to be a universal connection would greatly alter the internal processing operations architecture of the Margulis system because of the need for additional processing elements. More specifically, the Examiner's suggested modification would require the use of additional global interfaces at other locations (e.g., between the DOP 230 and image modulator 245, and between the image modulator 245 and the display screen 260). These additional interfaces would be required because once the DIP-DOP connection is made to be universal, all other interfaces in the system would likely need to be universal or the elements of the system would not be able to properly function together. As a result, significant additional hardware and/or software

would also be needed at all other elements of the system 200 resulting in significantly slower operations for the system 200.

Because the system 200 is intended to be a very high speed system, the change to a low-speed system would make the system unusable for its intended purpose (i.e., high-speed image processing operations). For these additional reasons, the Applicants assert that the proposed modification is non-obvious and that claim 9 is allowable over the proposed Margulis-Trovato combination.

Claims 11 and 12 are also Allowable Over the Proposed Combination

Claim 11 is an independent claim that recites a global interface and a presentation means the forms a final signal for display. Consequently, the Applicants assert that claim 11 is allowable for the same reasons as described above with respect to claim 9.

Claims 12 ultimately depends upon claim 11, which has been shown to be allowable above, and therefore, that claim is also allowable. In addition, it introduces additional content that, particularly when considered in context with the claim from which it depends, introduces additional incremental patentable subject matter. Accordingly, the Applicants reserve the right to present further arguments in the future with regard to this dependent claim if independent claim 9 is found to be unpatentable.

B) Claims 1-8 and 10 and 13 are Not Unpatentable under 35 U.S.C. §103(a) over Margulis in view of Trovato and Phillips

Claim 1 is an independent claim that recites a global interface and a presentation means the forms a final signal for display. Consequently, the Applicants assert that claim 1 is allowable for the same reasons as described above with respect to claim 9.

Claims 2-8 ultimately depend upon claim 1, claim 10 depends upon claim 9, and claim 13 depends upon claim 11, all of which has been shown to be allowable above, and therefore, these dependent claims are also allowable. In addition, they introduce additional content that, particularly when considered in context with the claims from which they

depend, introduce additional incremental patentable subject matter. Accordingly, the Applicants reserve the right to present further arguments in the future with regard to these dependent claims if independent claim 1, 9, and/or 11 are found to be unpatentable.

(8) Claims Appendix

Claim 1 (Previously presented): A digital television architecture, comprising:

a processing chassis operative to convert an analog input signal into at least a first digital signal for use in providing information to be provided to a user, the processing chassis including a dedicated power source and processing element;

a presentation chassis operative to convert audio and visual components of the at least first digital signal into a final signal for presentation on a display, the audio and visual conversion being performed in a first domain, the presentation device chassis being separate from the processing chassis and including a dedicated power source of the presentation chassis being different from the power source of the processing chassis; and

a global interface operative to provide a technology-independent communication path between the processing chassis and the presentation chassis.

Claim 2 (Original): The digital television of claim 1, wherein the interface includes a digital video interface.

Claim 3 (Original): The digital television of claim 1, wherein the processing chassis further includes an audio interface for converting audio signals contained within the input signal into a digital signal.

Claim 4 (Original): The digital television of claim 3, wherein the processing chassis further includes a video interface for converting the video signal contained within the input signal to high resolution digital signal.

Claim 5 (Original): The digital television of claim 1, wherein the processing chassis includes a power source and the presentation chassis includes a power source, the power source of the processing chassis providing power to the processing chassis independent of the power being supplied to the presentation chassis.

Claim 6 (Original): The digital television of claim 1, wherein the display device is a monitor.

Claim 7 (Original): The digital television of claim 1, wherein the input signal is provided to the processing chassis by one of the following:

a terrestrial antenna, a cable connection, and a satellite connection.

Claim 8 (Original): The digital television of claim 6, wherein the monitor is a CRT.

Claim 9 (Previously Presented): A modular television architecture, comprising:

a processing module including circuitry operative to convert an input signal from a first type into at least a second type, the conversion being performed in the digital domain;

a presentation module operative to convert audio and visual information contained within the at least second signal into a final signal for presentation on a display device, the audio and visual conversation being performed in a first domain, the presentation module being separate from and operating independently of the processing module; and

a global interface operative to provide a technology-independent communication path between the processing module and the presentation module.

Claim 10 (Original): The modular television of claim 9, wherein the processing module further includes a power source and a format converter and the presentation module further includes a power source, wherein the power source of the processing module is independent of the power source of the presentation module.

Claim 11 (Previously presented): A television system, comprising;

a processing module for providing signals that represent information to be provided on a suitable display device;

a presentation module including decoding and filtering elements, operative to process the signals provided by the processing module and display the images represented thereby on the display device, the presentation module being separate from and operating independently of the processing module; and

a global interface module for coupling the processing module and the presentation module together using a technology-independent path, wherein the processing and presentation modules operate independently from one another and the processing performed by the processing module is performed in the digital domain.

Claim 12 (Original): The system of claim 11, wherein the display device is a monitor.

Claim 13 (Original): The modular television of claim 11, wherein the processing module further includes a power source and a line doubler and the presentation module further includes a power source, wherein the power source of the processing module is independent of the power source of the presentation module.

(9) Evidence Appendix

Not Applicable.

(10) Related Proceedings Appendix

Not applicable.

In view of the foregoing, it is submitted that the application is in condition for allowance which is respectfully requested. The Commissioner is hereby authorized to charge any additional fees which may be required to Deposit Account No. 06-1135.

Respectfully submitted,

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